

MiniPC motherboard openEMS simulation & layout update

30 September 2026 | Actual 3-D FDTD | Python 3.12.14 | KiCad 10.0.6

Delivered: a connected routing candidate with local EM-guided changes. Actual openEMS simulations were run on the recovered stackup, a USB routing cutout and a core-power trace model. This report supersedes the earlier assumed-stackup impedance results. It is not full-board signal/power integrity signoff or proof that the MiniPC will operate.

Change / result	Verified outcome
USB3_SSRX P/N	112 trace segments: 0.150 to 0.140 mm. Nominal coupled edge gap becomes 0.135 mm; centerlines and lengths retained.
A10_0V9 top escapes	106 segments: 0.150 to 0.300 mm; 66.74 mm total copper length widened.
Layer stack	Recovered and restored 16-layer TU-883 stackup metadata.
Native KiCad DRC	0 unconnected; no new copper, drill, edge or thermal findings versus the preceding candidate.
Existing findings	1260 reported DRC findings remain; several categories are capped.
User manufacturing limits	3 mil trace/space minimum; all routing vias 18 mil pad / 8 mil drill.

What changed because of openEMS

At 2.5 GHz, the selected USB width gives **87.3-94.5 ohm** across two mask-profile models, versus 83.5-90.3 ohm before. The selected width balances those two modeled cases around 90 ohm. These are fixture-inclusive estimates, not fabricated-board impedance measurements.

For a 0.707 mm core-power trace model, the series-B inductance changes from **251.9 to 174.6 pH** at 2.5 GHz. Wider copper lowers the modeled local inductance; rail droop, current capacity and regulator stability were not established.

Open this candidate

MiniPC_openEMS-review.kicad_pcb with **MiniPC_openEMS-review.kicad_pro**. The openems-2026-09-30 folder contains reproducible scripts, CSX geometry, port time traces, spectra, logs and change manifests. The placed source and preceding routing candidates are preserved.

No original routed trace geometry was imported. The original Altium file was read only for its layer/material metadata. The fresh route remains the routing basis.

1. Recovered stackup and model boundaries

Board6/Data in the original MiniPC.PcbDoc records TU-883 dielectric with relative permittivity 3.6. The top and bottom mask each record 10 μm and relative permittivity 3.5. Outer copper is 45.001 μm ; all 14 internal copper layers are 17 μm . The recorded stack including mask totals 2.028002 mm, matching the imported 2.028 mm nominal thickness to rounding.

Copper layer, top to bottom	Copper (μm)	Dielectric below (mm)
F.Cu / Top	45.001	0.10
In1 / GND	17	0.10
In2 / Power	17	0.10
In3 / GND	17	0.12
In4 / Signal	17	0.12
In5 / Power	17	0.12
In6 / Signal	17	0.12
In7 / Power	17	0.12
In8 / GND	17	0.12
In9 / Signal	17	0.12
In10 / GND	17	0.12
In11 / Signal	17	0.12
In12 / GND	17	0.10
In13 / Power	17	0.10
In14 / GND	17	0.10
B.Cu / Bottom	45.001	-

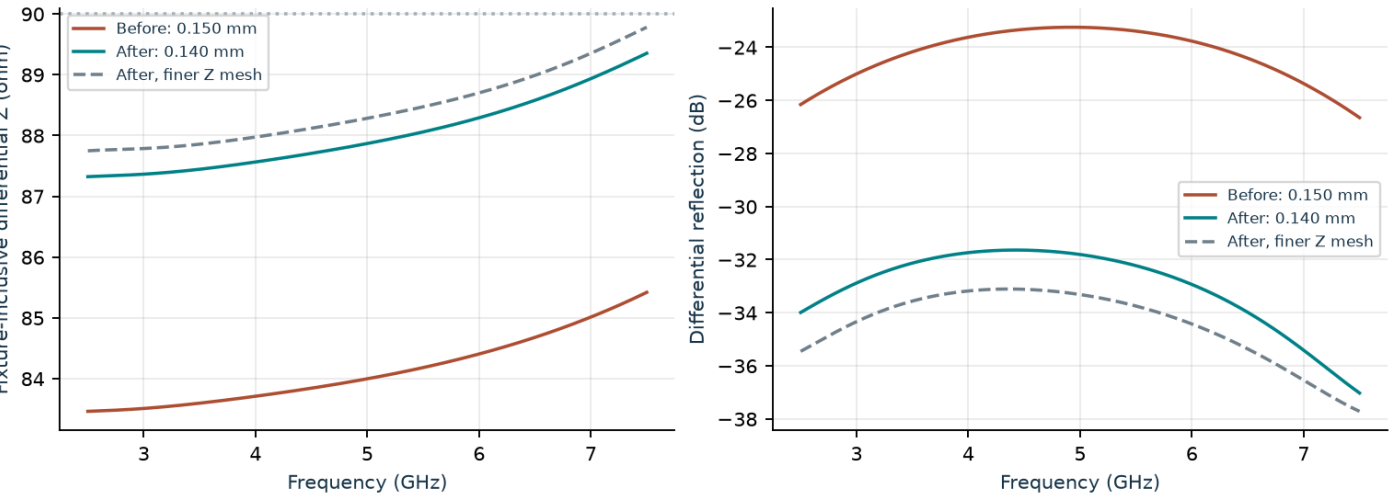
Known data versus assumptions. These are recorded design values, not a fabricator-approved finished stackup. Frequency-dependent D_k/D_f , etch tolerances, roughness, copper plating and detailed solder-mask profile remain unknown. KiCad loss-tangent fields are explicitly zero placeholders and are identified as unverified in the project text variables. Do not treat those zeros as material measurements.

The openEMS models use PEC copper with finite thickness and lossless dielectrics. The main models assume planarized mask filling to 10 μm above the traces; a conformal-mask sensitivity case is included. The top-layer reference is an ideal continuous adjacent GND plane. Full multilayer planes, apertures, coplanar pours, neighboring nets, packages and connectors are omitted.

The original file supplies stack metadata only. source-stackup.json and altium-stack-metadata.json retain the values and provenance. No old tracks or vias were copied.

2. Controlled-impedance comparison

FTDI AN_430 calls for nominal 90 ohm differential USB routing. [1] An 8 mm uniform coupled-line coupon uses the board pair's 0.275 mm center pitch, 0.100 mm dielectric spacing to GND, recorded material properties and finite copper thickness. Four grounded 45 ohm ports provide 90 ohm differential termination; equal and opposite input excitation is combined into differential waves.



At frequency	0.150 mm / 0.125 gap	0.140 mm / 0.135 gap
2.5 GHz: Re(Zdiff)	83.46 ohm	87.32 ohm
5.0 GHz: Re(Zdiff)	84.00 ohm	87.87 ohm
2.5 GHz: reflection	-26.16 dB	-33.99 dB

Zdiff is derived from the symmetric reciprocal coupon using $Z_{ref} \cdot \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}$, with $Z_{ref} = 90$ ohm. Lumped launch fixtures have not been de-embedded, so it is an approximate line-impedance estimate. The straight coupon has mirror-symmetric meshing and negligible common-mode incident contamination.

Mask profile determines the production width

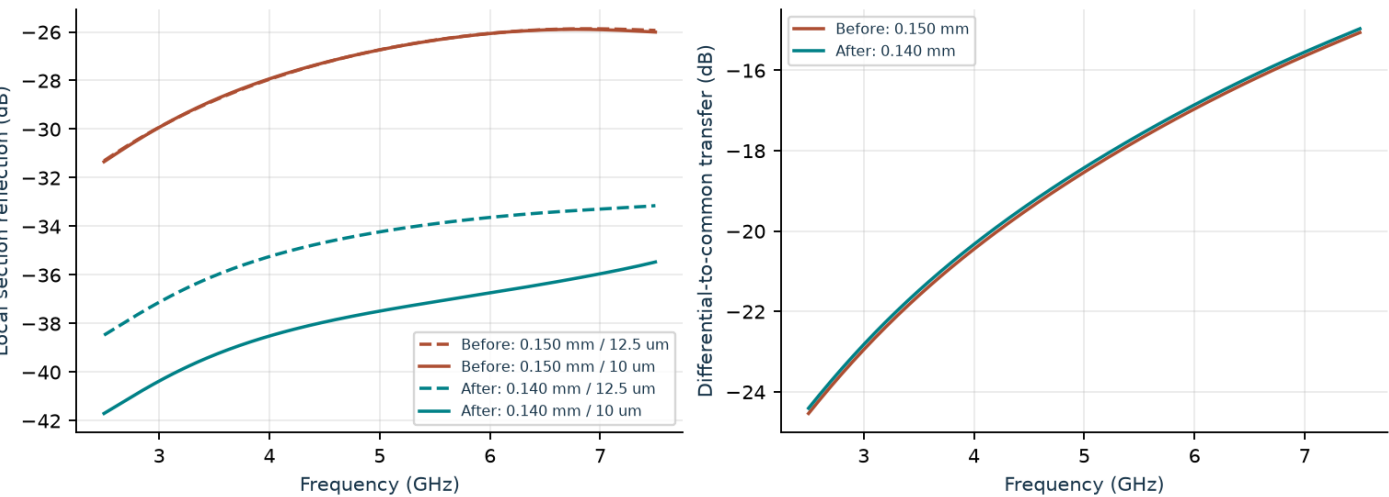
At 2.5 GHz, the 0.150 mm baseline gives 83.46 / 90.32 ohm for planarized / conformal mask. A 0.133 mm trial gives 90.07 / 97.40 ohm. The selected 0.140 mm width gives 87.32 / 94.46 ohm, balancing the two modeled profiles. Actual fabrication geometry is needed to select a final production width.

Halving the vertical mesh changes the selected-width result at 2.5 GHz by **0.43 ohm**. The 10 um transverse mesh resolves the selected trace with about 14 cells across its width. Finite launch effects make extracted impedance rise with frequency; this is not evidence of measured material dispersion.

The dedicated USB3_SSRX_openEMS net class stores 0.140 mm width and 0.135 mm nominal gap. The other USB/high-speed nets are not assigned this geometry because their layers and reference conditions differ. A global width change would not establish controlled impedance.

3. Actual routed USB section

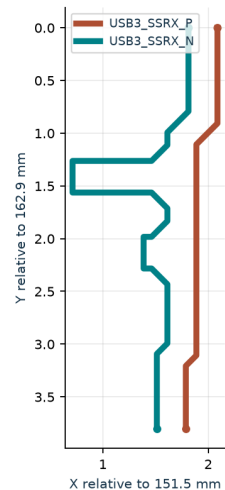
The modeled cutout follows the newly routed USB3_SSRX centerlines between board Y = 162.9 and 166.7 mm. It includes the two N-side tuning excursions. Width changes are applied to all 112 segments of this pair in the PCB; the cutout tests only this local portion. Connector fanout, through-hole stubs, package launches and the rest of the channel are outside the model.



10 um XY mesh	Before, 0.150 mm	After, 0.140 mm
Reflection at 2.5 GHz	-31.34 dB	-41.71 dB
Reflection at 5 GHz	-26.74 dB	-37.49 dB
Mode conversion at 5 GHz	-18.53 dB	-18.42 dB

Interpretation: the width decision is supported by the uniform-line impedance comparison. Deep reflection minima in the routed section are sensitive to grid alignment; the plotted mesh comparison must be considered before claiming a channel improvement. These results do not prove USB compliance or an improved eye diagram.

Actual local USB trace centerlines



Scope of the cutout

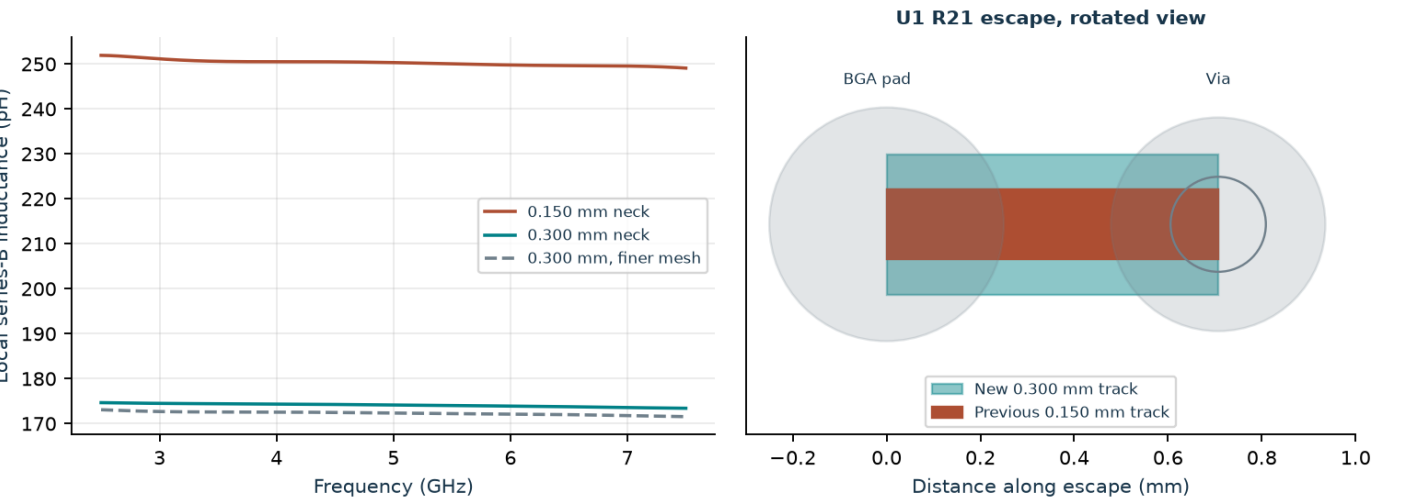
P/N centerline lengths: 3.924 / 5.824 mm. This partial section intentionally has unequal lengths because its tuning compensates geometry elsewhere in the full pair. Its common-mode transfer is therefore not the full-channel common-mode result.

The full pair retains matched geometric lengths of approximately 18.24293 mm. Electrical delay is not proven equal.

Actual underlying GND covers 100% / 98.63% of the P/N trace area in this cutout; the ideal continuous-plane model omits the small N-side aperture overlap and all coplanar copper.

4. Power interconnect and rail limitations

The local power model uses the 0.707107 mm centerline length of the top-layer A10_0V9 escape from U1 pad R21 toward its power via: (144.1951, 100.5642) to (143.6951, 101.0642) mm. Two 50 ohm grounded fixtures excite an isolated straight trace over the adjacent ideal GND plane. This is an EM interconnect comparison, not an energized 0.9 V rail simulation.



Local trace model	Before, 0.150 mm	After, 0.300 mm
$\text{Im}(B)/(2\pi f)$, 2.5 GHz	251.90 pH	174.62 pH
Finer transverse mesh, 2.5 GHz	-	173.05 pH
Isolated rectangular copper R, 20 C	1.806 milliohm	0.903 milliohm

The model gives a **30.7% reduction** in the local series-B inductance. Resistance is an independent calculation using copper resistivity 1.724e-8 ohm*m, not an openEMS loss result. Pads overlap much of the real escape, so the isolated rectangular resistance and modeled full-neck inductance are not the actual pad-to-plane parasitics. Via-barrel, spreading and return-path inductance are excluded.

After fixed-copper clearance screening, all 106 eligible top-layer A10_0V9 segments were widened to 0.300 mm. Native refill and DRC introduced no new copper, drill, edge or thermal findings. Track length, via placement and via dimensions are unchanged. This improves available copper cross-section without asserting a current rating.

Rail inventory retained from schematic/PCB audit	Nominal capacitance
A10_0V9: 104 x 100 nF, 24 x 100 uF, 4 x 330 uF	3730.4 uF
3V3: 15 direct capacitors	1476.3 uF
VDD_DDR / IO_1V8: direct 100 nF capacitors only	3.9 / 2.3 uF

Load profiles, capacitor bias/ESR/ESL, package/on-die models, regulator loop and remote-sense behavior, sequencing and thermal/current limits remain unverified. Bead-separated upstream capacitors are not included in the direct rail totals. Earlier ngspice droop scenarios remain hypothetical and are not relabeled as openEMS results.

5. Solver verification and reproducibility

openEMS was built from the official project sources and run through its Python 3.12.14 bindings. The accepted runs use Gaussian excitation centered at 5 GHz with 2.5 GHz bandwidth and a -50 dB field-energy termination criterion. Only 2.5-7.5 GHz spectra are retained for engineering comparisons; frequencies with weak excitation were excluded. All listed runs reached the energy criterion before the timestep cap.

Retained run	Cells	Timesteps	Final energy
Coupon before	1,152,086	44,525	-56.15 dB
Coupon after	1,148,290	44,928	-56.51 dB
Coupon after, finer Z	1,766,600	54,936	-50.85 dB
Routed cutout before	2,264,548	48,484	-54.65 dB
Routed cutout after	2,264,548	48,484	-54.65 dB
Power neck before	259,992	53,754	-58.52 dB
Power neck after	253,368	49,632	-64.07 dB
Power neck, finer X	501,768	58,565	-59.69 dB

Across retained models, the maximum summed normalized outgoing power is 1.001735 (numerical excess 0.173%). This is a consistency check, not a measurement of copper/dielectric loss. Maximum unintended common-mode incident amplitude is 0.0182% of differential incident amplitude. Differential simulations use balanced excitation and report its response column, not a full four-port S matrix.

For the routing cutout, changing XY cell size from 12.5 to 10 um changes complex differential reflection by at most 0.0015 before and 0.0068 after over the band. The power-neck transverse refinement changes the 2.5 GHz inductance estimate by 0.91%.

Reproduce and inspect

See **openems-2026-09-30/REPRODUCE.txt**. Each accepted model directory contains geometry.xml, model.json, port_ut/port_it time traces, sparameters.csv and results.json. accepted-results.json consolidates quality checks; layout-changes.json identifies every modified trace UUID. The XML, CSV, JSON and logs are retained for independent review.

Runtime: openems-2026-09-30/runtime/venv/bin/python. All CAD parsing and plotting also use Python 3.12. No Python 3.9 pcbnew/SWIG module is used. Native KiCad handles zone refill, board save and connectivity/DRC.

Source commits: openEMS 5b1ecb1244e6bd192d83efdf2bc84e5f83c96047; CSXCAD bd2c133392d93251b640da1f8e2367163f00b7f5. The official short smoke test was only an installation check. Rejected exploratory port setups and out-of-band results are excluded from accepted-results.json. [2-4]

Candidate PCB SHA-256:
e1e56b13565ad465e78f9d0299741d4061a4c4b8146b64bbc53aa9c314169043

6. DRC status, outstanding work and sources

Both the unchanged preceding candidate and this candidate report **1260 reported findings with identical category counts and zero unconnected items** in the same KiCad/library environment. No new copper, drill, edge or thermal findings were introduced. The capped 199-item mask-bridge sample changed among unchanged footprint pads; those raw differences are retained in drc-comparison.json. Footprints, pads, nets, placement, zone outlines and fixed drawings are unchanged. All trace centerlines and via geometry are preserved. The candidate has 14,988 segments, 3,140 vias, 1,052 footprints and 6,240 pads; 112 vias remain marked filled/capped. The placed source still has zero routing segments and vias.

Existing finding category	Reported count
Clearance (232 copper + 1 barcode)	233
Copper-to-hole clearance	1
Copper-to-board-edge clearance	4
Starved thermals	94
Solder-mask bridges (capped)	199
Malformed courtyards (capped)	199
Padstack warnings	18
Dangling track	1
Footprint library issues (capped)	199
Footprint library mismatches	4

Additional artwork/text findings remain in the complete DRC JSON. The reported total is not exhaustive where KiCad caps a category, and capped sample identities can change between runs. The retained dangling 3V3 track and inherited import findings are not hidden or waived.

Work required before fabrication release

Resolve the existing copper, hole, edge, mask and thermal findings. Confirm the schematic-to-PCB net mapping: the earlier audit found hierarchical names collapsing to common leaf labels; do not blindly update from the imported netlist. Close DDR4/PCIe and other interface constraints with endpoint topology, package delays, reference continuity and required operating speeds. The earlier total-copper screening found up to 31.86 mm spread in a DDR byte group; that is a flag for review, not a validated flight-time failure.

Obtain a fabricator-approved stackup, mask profile and frequency-dependent material data; verified connector/package/IBIS models; FPGA rail-current estimates and capacitor/VRM models. These are needed for complete channel, PDN, sequencing and thermal/current verification. This candidate is not fabrication-ready.

Primary sources

1. FTDI AN_430, FT60X PCB Layout Guidelines
2. Official openEMS project and source
3. openEMS ports and fixture limitations
4. openEMS S-parameter calculation
5. KiCad PCB stackup file format